REMARKS

In the Final Office Action, the Examiner noted that claims 1 and 3-21 are pending in the application, of which claims 20 and 21 are withdrawn from consideration. The Examiner rejected claims 1 and 3-21. By this response, claims 1 and 12 are amended and 20 and 21 remain withdrawn subject to possible rejoinder. In view of the above amendments and the following discussion, Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. Restriction Requirement

Applicants acknowledge the election of claims 1-19 (referred to as Group I).

II. Rejection of Claims Under 35 U.S.C. §102

The Examiner rejected claims 1 and 3-19 as being anticipated by Wang et al. (United States patent 6,594,809, issued July 15, 2003). More specifically, the Examiner stated that Wang teaches selecting a block of standard cells, associating a diode circuit with at least one input port of the cell block to form an augmented block, and implementing the augmented block. (Final Office Action, p. 3). The Examiner further stated that Wang teaches laying out components along with diode circuits associated with input ports and then routing conductors for connecting the components and connecting the input ports of the diode circuits. (Final Office Action, p. 8). The rejection is respectfully traversed.

Applicants have amended claim 1 to recite that the block of standard cells includes at least one primary input port, where each primary input port is a top-level input to the block that connects the block to additional circuitry. Support for the amendment is found in Applicants' specification, paragraph 0025. A diode circuit is then associated with each primary input port. Wang does not teach or suggest associating diode circuits with primary input ports of a block. Rather, Wang connects antenna diodes to conductors for which antenna rule violations were found during DRC. Wang connects antenna diodes to the conductors regardless of whether or not the conductors are primary inputs of a block. (Wang, col. 4, lines 1-38). There is no

explicit disclosure in Wang that antenna diodes are connected to top-level inputs of a block, as recited in Applicants' claim 1. Moreover, in Wang, it is not necessarily the case that each primary input of a block will be connected to an antenna diode.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Wang does not teach associating diode circuits with primary input ports of a block, Wang does not teach each and every element of Applicants' claim 1 as arranged therein. Accordingly, Wang does not anticipate Applicants' invention recited in claim 1. Claim 12 is amended to include features similar to those of claim 1 emphasized above. In Applicants' claim 14, diode circuits are associated with primary input ports of an embedded logic circuit, which is then placed, routed, and integrated with existing logic circuitry to form an integrated circuit. For the same reasons set forth above, Applicants contend that Wang does not anticipate the invention of claims 12 and 14.

Finally, claims 3-11, 13, and 15-19 depend, either directly or indirectly, from claims 1, 12, and 14 and recite additional features therefor. Since Wang does not anticipate Applicants' invention as recited in claims 1, 12, and 14, dependent claims 3-11, 13, and 15-19 are also not anticipated and are allowable. Therefore, Applicants contend that claims 1 and 3-19 are not anticipated by Wang and, as such, fully satisfy the requirements of 35 U.S.C. §102.

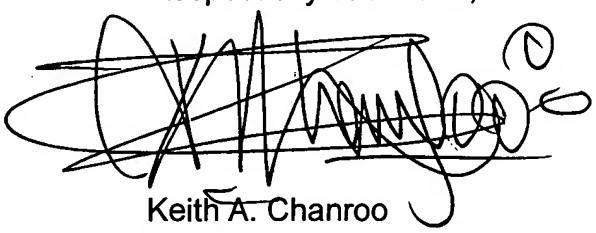
CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring the maintenance of any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Keith A. Chanroo at (408) 879-7710 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,



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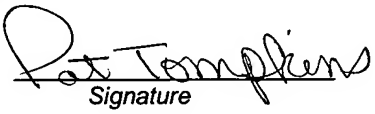
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on October ~~30~~ 02, 2006.

Pat Tompkins
Name



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